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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/809,416	03/26/2004	Chiaki Shinagawa	XA-10059	6810

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EXAMINER	
RUTZ, JARED IAN	

ART UNIT	PAPER NUMBER
2187	

DATE MAILED: 09/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/809,416	SHINAGAWA ET AL.	
	Examiner	Art Unit	
	Jared I. Rutz	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/26/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-16 as originally filed are pending in the instant application. Of these, there are 4 independent claims and 12 dependent claims.

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

3. The information disclosure statement (IDS) submitted on 3/26/04 is being considered by the examiner.

Specification

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: Nonvolatile memory wear leveling by data replacement processing.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. **Claims 2, 4, and 14** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

7. **Claim 2** recites the limitation "said memory area" in line 2. There is insufficient antecedent basis for this limitation in the claim. Claim 1 refers to "memory areas", "a first memory area", and "an unused second memory area".

8. **Claim 4** recites the limitation "said memory area" in line 2. There is insufficient antecedent basis for this limitation in the claim. Claim 1 refers to "memory areas", "a first memory area", and "an unused second memory area".

9. **Claim 14** recites the limitation "said memory area" in line 2. There is insufficient antecedent basis for this limitation in the claim. Claims 11 and 12 refer to "memory areas", "a used memory area", "a first memory area", and "an unused memory area".

Claim Rejections - 35 USC § 102

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

11. **Claims 1, 2, 4-6, 9, and 10** are rejected under 35 U.S.C. 102(e) as being anticipated by Chang et al. (US 2004/0080985).

12. **Claim 1** is taught by Chang as:

a. *A memory device comprising: an erasable and writable nonvolatile memory*. Non- volatile memory 124, discussed in paragraph 0047.

b. *And a control circuit*. Memory control system 128, discussed in paragraph 0048.

c. *Wherein said control circuit is enabled to perform replacement processing of memory areas at a prescribed timing*. Paragraph 0062 shows that the process of figure 2 can be performed when an initialization request is made.

d. *And wherein said replacement processing is accomplished by writing stored data in a first memory area in which rewriting is relatively infrequent into an unused second memory area*. Paragraph 0076-0077 explains how a block A with a low erase count compared to the average erase count, which shows that that block has been rewritten relatively infrequently, is moved into block B.

e. *And making the second memory area into which the writing has been done a used area in place of said first memory area*. Paragraph 0078 shows that the block mapping table is updated to show that block B, which contains the data that was stored in block A, is used to store data.

13. **Claim 2** is taught by Chang as:

f. *The memory device according to claim 1, wherein said memory area holds rewrite frequency data.* Figure 2 shows that memory areas contain erase counts 214, which indicates how many times the block has been erased.

g. *And wherein said control circuit references rewrite frequency data obtained from each of a group of memory areas and searches them for said first memory area.* Paragraph 0115 shows that an average erase count may be calculated by summing all the erase counts and dividing by the number of erase counts. Paragraph 0073 shows that the erase count for a given block is compared to the average erase count to determine if that block has a relatively low number of erasures.

14. **Claim 4** is taught by Chang as:

h. *The memory device according to claim 1, wherein said memory area holds rewrite frequency data.* Figure 2 shows that memory areas contain erase counts 214, which indicates how many times the block has been erased.

i. *And wherein said control circuit references the rewrite frequency data to search for a memory area in which rewriting is more frequent than in said first memory area and to make it said second memory area.* Paragraph 0076 shows that block B, the second memory area, is selected from the most frequently erased block table.

15. **Claim 5** is taught by Chang as:

j. *The memory device according to claim 1, wherein said control circuit performs said replacement processing in response to a specific command.* Paragraph 0062 shows that the process of figure 2 begins when an initialization request is made.

16. **Claim 6** is taught by Chang as:

k. *The memory device according to claim 1, wherein said control circuit performs said replacement processing in response to completion of processing of a specific command.* Paragraph 0062 shows that the initialization request may be initiated by a controller associated with the flash memory signal when a triggering condition is met. Accordingly, this shows that the replacement processing may occur when a specific command is completed, the command which caused the triggering condition to be met.

17. **Claim 9** is taught by Chang as:

l. *A memory device comprising: an erasable and writable nonvolatile memory.* Non- volatile memory 124, discussed in paragraph 0047.

m. *And a control circuit.* Memory control system 128, discussed in paragraph 0048.

n. *Wherein said control circuit is enabled to perform replacement processing of memory areas at a prescribed timing.* Paragraph 0062 shows that the process of figure 2 can be performed when an initialization request is made.

o. *And wherein said replacement processing is accomplished by replacing with a prescribed unused memory area a prescribed used memory area in which rewriting is less frequent than in the prescribed unused memory area.* Paragraph 0076-0077 explains how a block A with a low erase count compared to the average erase count, which shows that that block has been rewritten relatively infrequently, is moved into block B.

18. **Claim 10** is taught by Chang as:

p. *A memory device comprising: an erasable and writable nonvolatile memory.* Non- volatile memory 124, discussed in paragraph 0047.

q. *And a control circuit.* Memory control system 128, discussed in paragraph 0048.

r. *Wherein said control circuit is enabled to perform replacement processing of memory areas at a prescribed timing.* Paragraph 0062 shows that the process of figure 2 can be performed when an initialization request is made.

s. *And wherein said replacement processing is accomplished by replacing a prescribed memory area with another in which rewriting is less frequent than that prescribed memory area.* Paragraph 0076-0077 explains how a block A with a low erase count compared to the average erase count, which shows that that block has been rewritten relatively infrequently, is moved into block B.

t. *And placing said other memory area in an unused state while said prescribed memory area after the replacement is being used.* Paragraph 0078

shows that the block mapping table is updated to show that block B, which contains the data that was stored in block A, is used to store data.

Claim Rejections - 35 USC § 103

19. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

20. **Claim 3** is rejected under 35 U.S.C. 103(a) as being unpatentable over Chang (cited supra) in view of Estakhri et al. (US 6,145,051).

21. **Claim 3** is taught by Chang as shown supra with respect to claim 1.

22. Chang does not expressly disclose using a flag to indicate if an area is unused.

23. with respect to claim 3, Estakhri teaches:

u. *The memory device according to claim 1, wherein said nonvolatile memory is provided in each of its memory areas with a storage area for a distinguishing flag indicating whether or not the area is unused.* Column 5 lines 51-56 show that each memory location contains a used/free flag 112.

v. *And wherein said control circuit references said distinguishing flag to search for said unused second memory area.* Column 6 lines 10-15 show that

when data is to be written, the system locates a block having its used/free flag unset, which shows that the block is erased.

24. Chang and Estakhri are analogous art because they are from the same field of endeavor, non-volatile memory management systems.

25. At the time of the invention, it would have been obvious to one of ordinary skill in the art to use a flag to indicate if a block of a non-volatile memory has been used.

26. The motivation for doing so would have been to avoid the overhead of an erase before write cycle as stated by Estakhri at column 8 lines 25-29.

27. Therefore, it would have been obvious to combine Estakhri with Chang for the benefit of reducing overhead on write operations to obtain the invention as specified in **claim 3**.

28. **Claim 7** is rejected under 35 U.S.C. 103(a) as being unpatentable over Chang (cited supra) in view of Bruce et al. (US 6,000,006)

29. **Claim 7** is taught by Chang as shown supra with respect to claim 1

30. Chang does not expressly disclose giving priority to a command received during wear leveling.

31. With respect to claim 7, Bruce teaches:

w. *The memory device according to claim 1, wherein, in the event of an instruction by another command after a start of said replacement processing, the ongoing replacement processing is abandoned to give priority to processing of*

that other command. Column 12 lines 57-59 shows that wear leveling operations should be performed as background requests, giving host requests higher priority.

32. Chang and Bruce are analogous art because they are from the same field of endeavor, the design of flash memory control systems.

33. At the time of the invention it would have been obvious to one of ordinary skill in the art to perform wear leveling as a background process.

34. The motivation for doing so would have been to improve the latency of host requests, Bruce column 12 lines 59-60.

35. Therefore it would have been obvious to combine Bruce with Chang for the benefit of reducing latency on host requests to obtain the invention as specified in **claim 7**.

36. **Claim 8** is rejected under 35 U.S.C. 103(a) as being unpatentable over Chang (cited supra) in view of Bruce et al. (cited supra)

37. **Claim 8** is taught by Chang as shown supra with respect to claim 1.

38. Chang does not expressly disclose performing wear leveling when a certain number of writes has been performed.

39. With respect to claim 8, Bruce teaches:

x. *The memory device according to claim 1, wherein said control circuit performs said replacement processing in response to arrival of a frequency of*

rewriting into the nonvolatile memory at a prescribed number of times. Column 7 lines 34-45 discusses how thresholds are used to determine when a block needs to be moved to another location. When a block has exceeded the write threshold, it is moved to another location having fewer writes.

40. Chang and Bruce are analogous art because they are from the same field of endeavor, the design of flash memory control systems.

41. At the time of the invention it would have been obvious to one or ordinary skill in the art to use a write threshold as taught by Bruce to determine when to swap physical blocks as taught by Chang.

42. The motivation for doing so would have been to delay the start of wear leveling, therefore reducing system overhead in the early years of the system as taught by Bruce at column 12 lines 30-35.

43. Therefore it would have been obvious to combine Bruce with Chang for the benefit of reducing system overhead in the early years of a system to obtain the invention as specified in **claim 8.**

44. **Claims 11-16** are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang (cited supra) in view of Estakhri et al. (cited supra).

45. **Claim 11** is taught by Chang as:

y. *A memory device comprising: an erasable and writable nonvolatile memory*. Non- volatile memory 124, discussed in paragraph 0047

z. *And a control circuit.* Memory control system 128, discussed in paragraph 0048.

aa. *And is enabled to perform replacement processing at a prescribed timing on the used memory area indicated by said distinguishing flag.* Paragraph 0062 shows that the process of figure 2 can be performed when an initialization request is made.

bb. *And wherein said replacement processing is accomplished by writing stored data in a first memory area in which rewriting is relatively infrequent into an unused second memory area.* Paragraph 0076-0077 explains how a block A with a low erase count compared to the average erase count, which shows that that block has been rewritten relatively infrequently, is moved into block B.

cc. *And making the second memory area into which the writing has been done a used area in place of said first memory area.* Paragraph 0078 shows that the block mapping table is updated to show that block B, which contains the data that was stored in block A, is used to store data.

46. Chang does not expressly disclose the use of a flag to indicate unused memory areas.

47. With respect to claim 11, Estakhri teaches:

dd. *Wherein said nonvolatile memory has an unused area distinguishing table for storing a distinguishing flag which indicates whether or not any memory area is an unused area.* Column 5 lines 51-55 shows that there is a used/free flag for each memory location.

ee. *Wherein said control circuit, in write processing, makes one of the unused memory areas indicated by said distinguishing flag the destination for data writing.* Figure 9 item 202 shows that when the system wants to write to the non-volatile memory, a block with an unset used/free flag is located.

48. At the time of the invention it would have been obvious to one of ordinary skill in the art to use used/free flags to indicate available memory locations.

49. The motivation for doing so would have been to allow the system to determine which memory locations are available when the system is powered up, Estakhri column 6 lines 49-61.

50. Therefore, it would have been obvious to combine Estakhri with Chang for the benefit of determining used and unused memory locations at power up to obtain the invention as specified in **claims 11-16.**

51. **Claim 12** is taught by Chang as:

ff. *The memory device according to claim 11, wherein said nonvolatile memory has a used address registration table for registering, matched with logical addresses, physical addresses of memory areas to be used.* Paragraph 0080 shows block mapping table 462 of figure 5a, which associates LBAs with PBAs.

gg. *And wherein said control circuit, when altering the distinguishing flag to an unused area, invalidates the matching between the memory area allocated to the distinguishing flag and the physical address and, when altering the distinguishing*

flag to a used area, matches the memory area allocated to the distinguishing flag with a prescribed physical address. Paragraph 0078 shows that the block mapping table is updated when replacement processing is performed. This inherently involves matching the LBN to the PBN of the new block and making the LBN not point to the PBN of the old block, as this mapping is necessary to allow the system to access the written data.

52. **Claim 13** is taught by Estakhri as:

hh. *The memory device according to claim 12, wherein said control circuit, when it is to replace one memory area with another memory area to alter it into a used area, performs processing, before causing the matching between the logical address and the physical address pertaining to that alteration to be reflected in the used address registration table on said nonvolatile memory, to cause the distinguishing flag for said one memory area to be altered from an unused area to a used area to be reflected in the unused area distinguishing table on said nonvolatile memory.* Column 7 lines 50-56 show that when a write is performed, an empty block is found, and the data is written into that block and the used/free flag is set in step 206 of figure 9. This occurs before the map that correlates the logical addresses to the physical addresses is updated in step 212 of figure 9.

ii. *And performs processing after the matching has been reflected in said used address registration table, to cause the distinguishing flag for said other*

memory area to be altered from a used area into an unused area to be reflected in the unused area distinguishing table on said nonvolatile memory. If the write updates a previously written block, column 7 line 65 through column 8 line 7 shows that the old/new flag in the old block is set in step 210 of figure 9, which is before step 212. However, the used/free flag for the old block is not unset. Used /free flags are not unset until the system is unable to locate a block in which the used/free flag is set, step 202, and the system erases the flags and data for all blocks having a set old/new flag and an unset defect flag. This processing would occur for the other memory area after the logical to physical block mapping table had been updated to reflect the write to the new block.

53. **Claim 14** is taught by Chang as:

jj. *The memory device according to claim 12, wherein said memory area holds rewrite frequency data.* Figure 2 shows that memory areas contain erase counts 214, which indicate how many times the block has been erased.

kk. *And wherein said control circuit references rewrite frequency data obtained from each of a group of memory areas and searches them for said first memory area.* Paragraph 0115 shows that an average erase count may be calculated by summing all the erase counts and dividing by the number of erase counts. Paragraph 0073 shows that the erase count for a given block is compared to the average erase count to determine if that block has a relatively low number of erasures.

54. **Claim 15** is taught by Chang as:

ll. *The memory device according to claim 12, wherein said control circuit references said distinguishing flag to search for said unused second memory area.* Paragraph 0076 shows that block B, the second memory area, is selected from the most frequently erased block table.

55. **Claim 16** is taught by Chang as:

mm. *The memory device according to claim 12, wherein said control circuit references the rewrite frequency data to search for a memory area in which rewriting is more frequent than in said first memory area and to make it said second memory area.* Paragraph 0076 shows that block B, the second memory area, is selected from the most frequently erased block table if block A, the first memory area, is low compared to the average erase count.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jared I. Rutz whose telephone number is (571) 272-5535. The examiner can normally be reached on M-F 8:00 AM - 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jared I Rutz
Examiner
Art Unit 2187

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SUPERVISORY PATENT EXAMINER